

# DEBRA MARTIN

INTEGRATED CIRCUIT LAYOUT CONSULTANT

## CONTACT



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### WEB

[debramartin.com/layout](http://debramartin.com/layout)

## RECOMMENDATIONS

*"Her questions reveal her intelligent approach to her work and she often discovers and corrects problems that others overlook."*

Joe Sousa  
Staff Engineer  
Linear Technology Corporation

*"I was impressed by her meticulous work and her ability to solve problems...  
...sharp focus on cost effective workflow practices."*

Alfonso Centuori  
Chief Executive Officer  
iLABS Società a Responsabilità Limitata

*"Debra hit the ground running, laying out circuits within a day of her arrival."*

*...very easy to work with... great attention to detail, and takes pride in her work."*

Larry Kushner  
Principal Engineering Fellow  
Raytheon Technologies Corporation

## EDUCATION

### AAS ELECTRONICS

Community College of Rhode Island

### AAS INSTRUMENTATION

Community College of Rhode Island

## SUMMARY

20+ year veteran of semiconductor layout continually learning innovative methodologies and layout concepts. Self directed with the ability to make decisions based on problem analysis and evaluation of alternatives, risks, and consequences. Experience includes:

Full-custom, start-to-finish bipolar, CMOS, and BICMOS chip layouts

PMIC layout team leader

Finfet layout methodology development

SKILL pcell development for custom CMOS logic cells

Detail oriented craftsman possessing a firm understanding of masking layers with respect to device formation and parasitics. Able to recognize failure-prone layout structures and produce electrically robust mask sets. Excellent communicator with strong organizing and planning skills.

## HISTORY

### LAYOUT CONSULTANT, DEBRA MARTIN

CHELMSFORD MA/LAKEWOOD RANCH FL

9/2011- present

#### Client: Intrinsix Corp Marlborough MA

Layout Lead - multiple full test chip projects on GF 55nm BCDLITE process for clients with medical applications. (Bryan Allison)

#### Client: Analog Devices Incorporated Chelmsford MA

Prepare GaN and GaAs reticles and bonding diagrams for Hittite group (Rob Norton)

Facilitate integration of and provide support and training for CLIOSOFT SOS and KEYSIGHT ADS programs. (Anartya Mandal, Bob Broughton)

#### Client: IDEX America Incorporated Tewksbury MA

RXMUX layout for 65nm fingerprint scanner test chip. (Brian Jones)

#### Client: BAE Systems Incorporated Merrimack NH

Multiple layout blocks for production chip on 180nm SOI process (Larry Kushner)

#### Client: Analog Devices Incorporated Wilmington MA

Various 65nm blocks for PLL (Jim Dispirito)

#### Client: Analog Devices Incorporated Cambridge MA

Various 65nm blocks for probability processor chip for Lyric Labs group (Alex Alexeyev)

### SENIOR MASK DESIGNER, CAVIUM INCORPORATED

NORTHBOROUGH MA

10/2013-3/2015

Methodology development for GF and Samsung 14nm finfet layout processes

Various 14nm finfet blocks (VCO, Phase Detector, Divider, Charge Pump, Loop Filters) for PLL portion of SERDES chip

### SENIOR MASK DESIGNER, LINEAR TECHNOLOGY CORPORATION

CHELMSFORD MA

3/2001-8/2011

Plan, organize, execute, and verify full chip layouts

LTC4088 iPhone 3G battery charger layout team leader

Full chip CMOS PMIC layouts with circuits such as precision bandgaps, oscillators, amplifiers, comparators, custom logic, and various power switch and routing topologies

Independently created Cadence SKILL PCELL library for stackable logic cells

Precision op-amps and switching regulators on bipolar processes